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APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

A CIRCUIT TO ADD AND SUBTRACT TWO DIFFERENTIAL SIGNALS

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A CIRCUIT TO ADD AND SUBTRACT TWO DIFFERENTIAL SIGNALS

BACKGROUND OF THE INVENTION

[0001] An electrical circuit to simultaneously add and subtract two differential input signals may have different uses, such as, for example, in radio frequency (RF) applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Embodiments of the invention are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like reference numerals indicate corresponding, analogous or similar elements, and in which:

[0003] FIG. 1 shows an exemplary block diagram in accordance with some embodiments of the invention;

[0004] FIG. 2 shows an exemplary electrical circuit including reactive elements in accordance with some embodiments of the invention;

[0005] FIG. 3 shows an alternate exemplary electrical circuit including reactive elements in accordance with some embodiments of the invention;

[0006] FIG. 4 shows an exemplary electrical circuit including transmission lines in accordance with some embodiments of the invention;

[0007] FIG. 5 shows an alternate exemplary electrical circuit including transmission lines in accordance with some embodiments of the invention; and

[0008] FIG. 6 is a simplified block-diagram illustration of an exemplary communication system, in accordance with some embodiments of the present invention;

[0009] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0010] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of embodiments of the invention. However it will be understood by those of ordinary skill in the art that the embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the embodiments of the invention.

[0011] It should be understood that the present invention may be used in a variety of applications. Although the present invention is not limited in this respect, the circuits disclosed herein may be used in many apparatuses such as the transmitters and receivers of a radio system. Radio systems intended to be included within the scope of the present invention include, by way of example only, cellular radio telephone communication systems, wireless local area networks that meet the existing 802.11a, b, g, and future high data-rate versions of the above, two-way radio communication systems, one-way pagers, two-way pagers, personal communication systems (PCS), Bluetooth wireless communication systems, Zigbee wireless communication systems and the like.

[0012] Types of cellular radiotelephone communication systems intended to be within the scope of the present invention include, although not limited to, Direct Sequence - Code Division Multiple Access (DS-CDMA) cellular radiotelephone communication systems, Global System for Mobile Communications (GSM) cellular radiotelephone systems, North American Digital Cellular (NADC) cellular radiotelephone systems, Time Division Multiple Access (TDMA) systems, Extended-TDMA (E-TDMA) cellular radiotelephone systems, wideband CDMA (WCDMA), General Packet Radio Service (GPRS) systems, Enhanced Data for GSM Evolution (EDGE) systems, 3.5G and 4G systems.

[0013] FIG. 1 shows an exemplary block diagram including an electrical circuit 2 in accordance with some embodiments of the invention. Exemplary electrical circuit 2 may include a differential sum/difference block 4, signal sources 6 and 8, and load elements 10 and 12. Differential sum/difference block 2 may include terminals 14, 16, 18, 20, 22, 24, 26 and 28.

[0014] Signal source 6 may have terminals 30 and 32, and may have an output impedance Z_a between terminals 30 and 32, as described in equation (1):

(1) $Z_a = (a_1 + ja_2), \quad a_1 \geq 0,$

where j denotes the square root of minus one, a_1 is the real component of output impedance Z_a and a_2 is the imaginary component of output impedance Z_a.

[0015] In addition, signal source 6 may generate a differential signal $S_A(t)$ between terminals 30 and 32, having the general form described in Equation (2):

(2) $$S_A(t) = A_A(t) \cdot e^{j2\pi f_A(t)t + j\theta_A(t)}$$

where $A_A(t)$ is the amplitude, $f_A(t)$ is the frequency and $\theta_A(t)$ is the initial phase of the differential signal $S_A(t)$, and t is a time variable.

[0016] Signal source 8 may have terminals 34 and 36, and may have an output impedance Z_b between terminals 34 and 36, as described in equation (3):

(3) $Z_b = (b_1 + jb_2), \quad b_1 \geq 0,$

where b_1 is the real component of output impedance Z_b and b_2 is the imaginary component of output impedance Z_b.

[0017] In addition, signal source 8 may generate a differential signal $S_B(t)$ between terminals 34 and 36, having the general form described in Equation (4):

(4) $$S_B(t) = A_B(t) \cdot e^{j2\pi f_B(t)t + j\theta_B(t)}$$

where $A_B(t)$ is the amplitude, $f_B(t)$ is the frequency and $\theta_B(t)$ is the initial phase of the differential signal $S_B(t)$.

[0018] Load element 10 may have terminals 38 and 40, and may have an input impedance Z_c between terminals 38 and 40, as described in equation (5):

(5) $Z_c = (c_1 + jc_2)$, $c_1 \geq 0$,

where c_1 is the real component of output impedance Z_c and c_2 is the imaginary component of output impedance Z_c.

[0019] Similarly, load element 12 may have terminals 42 and 44, and may have an input impedance Z_d between terminals 42 and 44, as described in equation (6):

(6) $Z_d = (d_1 + jd_2)$, $d_1 \geq 0$,

where d_1 is the real component of output impedance Z_d and d_2 is the imaginary component of output impedance Z_d.

[0020] Terminals 14 and 16 of a first differential input port of differential sum/difference block 2 may be connected to terminals 30 and 32, respectively. Terminals 18 and 20 of a first differential output port of differential sum/difference block 2 may be connected to terminals 40 and 38, respectively. Terminals 22 and 24 of a second differential output port of differential sum/difference block 2 may be connected to terminals 42 and 44, respectively. Terminals 26 and 28 of a second differential input port of differential sum/difference block 2 may be connected to terminals 36 and 34, respectively.

[0021] Although the present invention is not limited in this respect, signal sources 4 and 6 may have substantially equal output impedances, as shown in equation (7):

(7) $Z_b \approx Z_a = (a_1 + ja_2) \quad a_1 \geq 0$,

and load elements 8 and 10 may have substantially equal input impedances, as shown in equation (8):

(8) $Z_d \approx Z_c = (c_1 + jc_2) \quad c_1 \geq 0$.

Furthermore, the frequency of differential signal $S_A(t)$ may be substantially equal to the frequency of differential signal $S_B(t)$, as shown in equation (9):

(9) $f_A(t) \approx f_B(t)$.

[0022] Moreover, the output impedance of signal sources 6 and 8 may be substantially active, as shown in equation (10):

(10) $a_1 >> |a_2|$,

and the input impedance of load elements 10 and 12 may be substantially active, as shown in equation (11):

(11) $c_1 >> |c_2|$.

[0023] Differential sum/difference block 4 may output a differential signal $S_C(t)$ at terminals 20 and 18, that may be substantially proportional to the sum of signals $S_A(t)$ and $S_B(t)$, as shown in equation (12):

(12) $$S_C(t) \approx K_1 \cdot \{S_A(t) + S_B(t)\} \cdot e^{j\frac{\pi}{2}\frac{f(t)}{f_0}},$$

where K_1 is a coefficient of proportionality, and f_0 is a center frequency of $f_A(t)$.

[0024] Furthermore, differential sum/difference block 4 may output a differential signal $S_D(t)$ between terminals 22 and 24 that may be substantially proportional to the difference between signals $S_A(t)$ and $S_B(t)$, as shown in equation (13):

(13) $$S_D(t) \approx K_2 \cdot \{S_A(t) - S_B(t)\} \cdot e^{j\frac{\pi}{2}\frac{f(t)}{f_0}},$$

where K_2 is a coefficient of proportionality.

Consequently differential sum/difference block 4 may be considered a sum-difference combiner.

[0025] FIG. 2 shows an exemplary differential sum/difference block 104 in accordance with some embodiments of the invention. Differential sum/difference block 104 may be implemented or partially implemented in an integrated circuit assembled on a printed circuit board 100. Those elements of differential sum/difference block 104 that are not implemented in the integrated circuit (which may be all elements of differential sum/difference block 104) may be implemented in

the packaging of the integrated circuit, as discrete components assembled on printed circuit board 100, as part of printed circuit board 100, or any combination thereof.

[0026] Differential sum/difference block 104 may include lumped reactive elements 106, 108, 110, 112, 114, 116, 118 and 120, having physical dimensions that are significantly smaller than the wavelength $\lambda_A(t)$ that is associated with frequency $f_A(t)$. (The wavelength $\lambda_A(t)$ may be the wavelength of a signal at frequency $f_A(t)$ in a material having an effective electrical permeability similar to that of a lumped reactive element.) Reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may have a substantially equal impedance Z_e, as described in equation (14):

$$(14) \quad Z_e = (e_1 + je_2), \qquad e_1 \geq 0$$

where e_1 is the real component of impedance Z_e and e_2 is the imaginary component of impedance Z_e.

[0027] Differential sum/difference block 104 may include lumped reactive elements 122, 124, 126 and 128, having physical dimensions that are significantly smaller than the wavelength $\lambda_A(t)$. Reactive elements 122, 124, 126 and 128 may have a substantially equal impedance Z_f, as described in equation (15):

$$(15) \quad Z_f = (f_1 + jf_2), \qquad f_1 \geq 0$$

where f_1 is the real component of impedance Z_f and f_2 is the imaginary component of impedance Z_f.

[0028] Reactive elements 106, 118 and 122 may be connected to terminal 14.

[0029] Reactive elements 108, 120 and 122 may be connected to terminal 16.

[0030] Reactive elements 116, 120 and 128 may be connected to terminal 18.

[0031] Reactive elements 114, 118 and 128 may be connected to terminal 20.

[0032] Reactive elements 106, 110 and 124 may be connected to terminal 22.

[0033] Reactive elements 108, 112 and 124 may be connected to terminal 24.

[0034] Reactive elements 110, 116 and 126 may be connected to terminal 26.

[0035] Reactive elements 112, 114 and 126 may be connected to terminal 28.

[0036] According to a first exemplary embodiment of the invention, reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may have substantially inductive impedances, and reactive elements 122, 124, 126 and 128 may have substantially capacitive impedances, as shown in equations (16) and (17) respectively:

(16) $Z_e = (e_1 + je_2)$, $\quad e_1 \geq 0 , e_2 \geq 0 , e_1 << | e_2 |$

(17) $Z_f = (f_1 + jf_2)$ $\quad f_1 \geq 0 , f_2 \leq 0 \ , \ f_1 << | f_2 |$

Moreover, the impedance of reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may be substantially twice as much as the impedance of reactive elements 122, 124, 126 and 128, as shown in equation (18):

(18) $e_2 \approx 2 | f_2 |$.

[0037] Furthermore, although the scope of the present invention is not limited in this respect, the impedance of reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may be related to the impedances of signal sources 6 and 8 and to the impedances of load elements 10 and 12, as shown in equation (19):

(19) $e_2 \approx \sqrt{2a_1 \cdot c_1}$.

Similarly, the impedance of reactive elements 122, 124, 126 and 128 may be related to the impedances of signal sources 6 and 8 and to the impedances of load elements 10 and 12, as shown in equation (20):

(20) $f_2 \approx -\sqrt{\frac{a_1 \cdot c_1}{2}}$.

[0038] Differential signal $S_C(t)$ may be substantially proportional to the sum of $S_A(t)$ and $S_B(t)$, as shown in equation (12), and differential signal $S_D(t)$ may be substantially proportional to the difference between $S_A(t)$ and $S_B(t)$, as shown in equation (13).

[0039] According to a second exemplary embodiment of the invention, reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may have substantially capacitive impedances, and reactive elements 122, 124, 126 and 128 may have substantially inductive impedances, as shown in equations (21) and (22) respectively:

(21) $Z_e = (e_1 + je_2), \qquad e_1 \geq 0, e_2 \leq 0, e_1 << |e_2|$

(22) $Z_f = (f_1 + jf_2), \qquad f_1 \geq 0, f_2 \geq 0 \;, f_1 << |f_2|.$

The impedance of reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may be substantially twice as much as the impedance of reactive elements 122, 124, 126 and 128, as shown in equation (23):

(23) $f_2 \approx 2|e_2|.$

[0040] Furthermore, although the scope of the present invention is not limited in this respect, the impedance of reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may be related to the impedances of signal sources 6 and 8 and the impedances of load elements 10 and 12, as shown in equation (24):

(24) $e_2 \approx -\sqrt{2a_1 \cdot c_1}$.

Similarly, the impedance of reactive elements 122, 124, 126 and 128 may be related to the impedances of signal sources 6 and 8 and the impedances of load elements 10 and 12, as shown in equation (25):

(25) $f_2 \approx 2\sqrt{2a_1 \cdot c_1}$.

[0041] Differential signal $S_C(t)$ may be substantially proportional to the sum of $S_A(t)$ and $S_B(t)$, as shown in equation (12), and differential signal $S_D(t)$ may be substantially proportional to the difference between $S_A(t)$ and $S_B(t)$, as shown in equation (13).

[0042] The second embodiment, described above, may be modified to include center taps 130, 132, 134 and 136 for reactive elements 122, 124, 126 and 128, respectively. Center taps 130, 132, 134 and 136 may be optionally connected to a supply or a supply return signal (not shown).

[0043] In both the first and second exemplary embodiments, a non-exhaustive list of examples for the reactive elements having substantially capacitive impedances includes a surface mounted device (SMD) capacitor located on a printed circuit board (PCB), a SMD capacitor located on a substrate of an integrated circuit (IC) device, a

through-hole capacitor, a metal-insulator-metal (MIM) capacitor, a metal-oxide semiconductor (MOS) capacitor, poly capacitor, and the like.

[0044] In both the first and second exemplary embodiments, a non-exhaustive list of examples for the reactive elements having substantially inductive impedances includes a SMD inductor located on a PCB, a SMD inductor located on a substrate of an IC device, a through-hole inductor, a planar on-chip inductor, and the like.

[0045] In the case of substantially inductive reactive elements having center taps, a non-exhaustive list of examples includes any combination of an SMD differential inductor located on a PCB, a SMD differential inductor located on a substrate of an IC device, a through-hole differential inductor, a planar on-chip differential inductor with a center tap, and the like.

[0046] FIG. 3 shows an alternate exemplary differential sum/difference block 105 in accordance with some embodiments of the invention. Differential sum/difference block 105 may be implemented or partially implemented in an integrated circuit assembled on a printed circuit board 101. Those elements of differential sum/difference block 105 that are not implemented in the integrated circuit (which may be all elements of differential sum/difference block 105) may be implemented in the packaging of the integrated circuit, as discrete components assembled on printed circuit board 101, as part of printed circuit board 101, or any combination thereof.

[0047] Differential sum/difference block 105 may include lumped reactive elements 106, 108, 110, 112, 114, 116, 118 and 120, as described hereinabove with respect to FIG. 2. The physical dimensions and impedances of reactive elements 106, 108, 110, 112, 114, 116, 118 and 120 may be as described hereinabove with respect to FIG. 2. Moreover, as described hereinabove with respect to FIG. 2, differential sum/difference block 105 may include center taps 130, 132, 134 and 136 for reactive elements 122, 124, 126 and 128, respectively. Center taps 130, 132, 134 and 136 may be optionally connected to a supply or a supply return signal (not shown).

[0048] Reactive elements 108, 118 and 122 may be connected to terminal 14.

[0049] Reactive elements 106, 120 and 122 may be connected to terminal 16.

[0050] Reactive elements 116, 120 and 128 may be connected to terminal 18.

[0051] Reactive elements 114, 118 and 128 may be connected to terminal 20.

[0052] Reactive elements 106, 110 and 124 may be connected to terminal 22.

[0053] Reactive elements 108, 112 and 124 may be connected to terminal 24.

[0054] Reactive elements 112, 114 and 126 may be connected to terminal 26.

[0055] Reactive elements 110, 116 and 126 may be connected to terminal 28.

[0056] FIG. 4 shows an exemplary distributed differential sum/difference block 204 in accordance with some embodiments of the invention. Differential sum/difference block 204 may be implemented on a printed circuit board 200 or any other suitable implementation.

[0057] Differential sum/difference block 204 may include distributed differential transmission lines 206, 208, 210 and 212, having physical dimensions substantially equal to one quarter of the wavelength $\lambda_A(t)$ (the wavelength $\lambda_A(t)$ may be the wavelength of a signal at frequency $f_A(t)$ in a material having an effective electrical permeability similar to that of a transmission line), and having a substantially equal impedance Z_h, as described in equation (26):

$$(26) \quad Z_h = (h_1 + jh_2), \qquad h_1 \geq 0, h_1 >> |h_2|$$

where h_1 is the real component of impedance Z_h and h_2 is the imaginary component of impedance Z_h.

[0058] Impedance Z_h may be related to the impedances of signal sources 4 and 6 and to the impedances of load elements 8 and 10, as shown in equation (27):

$$(27) \quad h_1 \approx \sqrt{2a_1 \cdot c_1}.$$

[0059] Distributed differential transmission line 206 may include a conductor 214 and a conductor 216. Distributed differential transmission line 206 may have terminals 218 and 220 connected to conductor 214, and may have terminals 222 and 224 connected to conductor 216. Terminals 218 and 222 may be associated with a first physical end of distributed differential transmission line 206, while terminals 220 and 224 may be associated with a second physical end of distributed differential transmission line 206.

[0060] Distributed differential transmission line 208 may include a conductor 226 and a conductor 228. Distributed differential transmission line 208 may have terminals

230 and 232 connected to conductor 226, and may have terminals 234 and 236 connected to conductor 228. Terminals 230 and 234 may be associated with a first physical end of distributed differential transmission line 208, while terminals 232 and 236 may be associated with a second physical end of distributed differential transmission line 208.

[0061] Distributed differential transmission line 210 may include a conductor 238 and a conductor 240. Distributed differential transmission line 210 may have terminals 242 and 244 connected to conductor 238, and may have terminals 246 and 248 connected to conductor 240. Terminals 242 and 246 may be associated with a first physical end of distributed differential transmission line 210, while terminals 244 and 248 may be associated with a second physical end of distributed differential transmission line 210.

[0062] Distributed differential transmission line 212 may include a conductor 250 and a conductor 252. Distributed differential transmission line 212 may have terminals 256 and 258 connected to conductor 250, and may have terminals 260 and 262 connected to conductor 252. Terminals 256 and 260 may be associated with a first physical end of distributed differential transmission line 212, while terminals 258 and 262 may be associated with a second physical end of distributed differential transmission line 212.

[0063] Terminals 218 and 244 may be connected to terminal 14.

[0064] Terminals 222 and 248 may be connected to terminal 16.

[0065] Terminals 224 and 258 may be connected to terminal 18.

[0066] Terminals 220 and 262 may be connected to terminal 20.

[0067] Terminals 234 and 242 may be connected to terminal 22.

[0068] Terminals 230 and 246 may be connected to terminal 24.

[0069] Terminals 236 and 256 may be connected to terminal 26.

[0070] Terminals 232 and 260 may be connected to terminal 28.

[0071] A non-exhaustive list of examples for distributed differential transmission lines 206, 208, 210 and 212 may include a differential micro-strip transmission line, a differential strip-line transmission line, a differential waveguide, a differential coaxial cable, and the like.

[0072] Differential signal $S_C(t)$ may be substantially proportional to the sum of $S_A(t)$ and $S_B(t)$, as shown in equation (12), and differential signal $S_D(t)$ may be substantially proportional to the difference between $S_A(t)$ and $S_B(t)$, as shown in equation (13).

[0073] FIG. 5 shows an alternate exemplary differential sum/difference block 205 in accordance with some embodiments of the invention. Differential sum/difference block 205 may be implemented on a printed circuit board 201 or any other suitable implementation.

[0074] Differential sum/difference block 205 may include distributed differential transmission lines 206, 208, 210 and 212, as described hereinabove with respect to FIG. 4. The physical dimensions and impedances of distributed differential transmission lines 206, 208, 210 and 212 may be as described hereinabove with respect to FIG. 4.

[0075] Terminals 222 and 248 may be connected to terminal 14.

[0076] Terminals 218 and 244 may be connected to terminal 16.

[0077] Terminals 224 and 258 may be connected to terminal 18.

[0078] Terminals 220 and 262 may be connected to terminal 20.

[0079] Terminals 234 and 242 may be connected to terminal 22.

[0080] Terminals 230 and 246 may be connected to terminal 24.

[0081] Terminals 232 and 260 may be connected to terminal 26.

[0082] Terminals 236 and 256 may be connected to terminal 28.

[0083] FIG. 6 is a simplified block-diagram illustration of an exemplary communication system, in accordance with some embodiments of the present invention. A communication device 402 is able to communicate with a communication device 404 over a communication channel 406. A transmitter according to embodiments of the present invention may be present in communication device 402 only or in communication device 404 only or in both communication devices 402 and 404. The following description is based on the example of a transmitter according to one or another of the embodiments of the present invention present in communication device 402 only, although the present invention is not limited in this respect.

[0084] Although the present invention is not limited in this respect, the communication system shown in FIG. 6 may be part of a cellular communication system, with one of communication devices 402, 404 being a base station and the other a mobile station or with both communication devices 402, 404 being mobile stations, a pager communication system, a personal digital assistant and a server, etc. Communication devices 402 and 404 may include antennas 408 and 410, respectively, which may be, for example, dipole antennas, loop antennas, shot antennas dual antennas, omni-directional antennas or any other suitable antennas.

[0085] Communication device 402 may include a transmitter 412 that may include a phase splitter 414, a differential sum/difference block 416 and a power amplifier 418. Phase splitter outphasing 414 may receive a differential signal 420 that may contain information to be transmitted, and may output differential phase shifted signals 422 and 424 having amplitudes substantially similar to the amplitude of signal 420. Differential phase shifted signal 424 may have a phase delay of substantially 90° relative to differential phase shifted signal 422.

[0086] Differential sum/difference block 416 may receive differential phase shifted signals 422 and 424 as inputs and may output a differential sum outphased signal 426, and a differential difference outphased signal 428.

[0087] Power amplifier 418 may receive differential sum outphased signal 426 and may amplify it, using for example, a first power amplifying element (not shown). Similarly, power amplifier 418 may receive differential difference outphased signal 428 and may amplify it, using for example, a second power amplifying element (not shown). Although the present invention is not limited in this respect, power amplifier 418 may combine these amplified signals by means of, for example, a transmission-line-combiner with reactive shunt terminations, and may output an RF signal 430 that may then be transmitted by antenna 408 over communication channel 406. Alternatively, the transmission-line-combiner may be replaced by a different combiner scheme, such as, for example, Hybrid BALUN or center-tap inductor.

[0088] Communication device 404 may include a receiver 432. Receiver 432 may receive a modulated data signal 434 from communication channel 406 via antenna 410, and may, for example, extract the information contained in signal 434 by, for example, downconverting and demodulating signal 434.

[0089] It will be appreciated by persons of ordinary skill in the art that communication devices 402 and 404, and in particular transmitter 412 and receiver 432, may include additional components that are not shown in FIG. 4 so as not to obscure the description of embodiments of the invention.

[0090] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the spirit of the invention.